ACORN FLOPPY DSC CONTROLLER BOARD

UNIT DESCRIPTION

CONTENTS

Written and Produced for Acorn Computers Limited by Arch Technical Publications Limited,
St, Lukes House, 5, Walsworth Road, Hitchin, Herts.

TABLES

FIGURES

1. INTRODUCTION

1.1 GENERAL

The Floppy Disc Controller Board provides an interface to one or two, single or double-sided floppy disc drive units. The board connects to the Acorn Bus and, via a ribbon cable, to the floppy disc drive; multiple floppy disc drives are daisy chained.

Throughout this document, the terms disc and disc drive refer respectively to the flexible plastic dise recording media ("floppy disc", "mini floppy", "flippy", etc) and to the unit containing the drive mechanism and read/write/control electronics into which the disc is inserted.

The board uses the 8271 programmable floppy disc controller device (FDC). The FDC is a high level controller that relieves the CPU of many tasks associated with floppy disc control. It supports a soft sectored format that is IBM 3740 compatible.

The Acorn Disc Operating System (DOS) provides comprehensive commands for the control of disc drives. This is available as ROM pre-programmed to suit a number of floppy disc drive types.

1.2 PRINCIPLES OF OPERATION

A block diagram of the Floppy Disc Controller Board is given on Figure 1.

The FDC executes each data record transfer, writing to or reading from the disc, in three phases. It accepts commands from the CPU, executes the command (transfers the data record byte by byte), and provides a result (e.g. transfer completed) at the end of the execution phase.

The FDC is controlled by the CPU using various command instructions. Each command is executed autonomously by the FDC. At the end of the execution phase, the FDC flags the CPU (NNMI) which reads the current states (result and status register) before issuing the next command.

Each command defines the mode of operation required, such as Initialization, Read Data, Write Data, etc. and may be supplemented by up to five parameter bytes which further define the command.

At power up or system reset (NRST), the FDC is reset. This halts any commands in progress, clears the registers, and forces the FDC into an idle state. The FDC can also be reset by software using a Reset Command.

The FDC is initialized using commands and parameters which specify the various disc drive characteristics such as step rate between tracks, head settling time (pause between final step signal to drive and the writing/reading of data), and head load time.

The head is loaded when a disc is selected, and remains in contact with the disc while stepping over the surface. The head load time is the time between head load and the writing/reading of data.

The final phase of initialization consists of setting the head(s) on each drive equipped to track 0 using *a* Seek Command. This command causes the FDC to locate the head of the first drive to track 0 and to interrupt the CPU which reads and resets the Result Register. The FDC then tests the second disc drive position. If a drive is present, its head is located to track 0 and the CPU interrupted to read and reset the Result Register for the second drive.

The locating of the head(s) to track 0 ensures that the head position is known, particularly after power up.

Each data transfer (write to or read from disc) consists of three phases. Each phase is initiated by the CPU with all further actions controlled by the FDC. These phases are:

COMMAND PHASE
The CPU addresses the FDC to enable its input and output buffers and the command and parameter registers as appropriate and transfers a command (Table 1) and from zero to five parameter instructions via the Data Bus, to the selected register. The FDC is addressed for each command or parameter transfer.

The command defines the type of transfer required and the parameters define the data, e.g. location (disc, surface, track, sector) and length of data record.

On completion of the Command Phase, the FDC enters the appropriate Execute Phase.

WRITE EXECUTE PHASE
During this phase, each byte of the data record to be written is loaded onto the Data Bus by the CPU and the NWDS signal set active to initiate the writing of that byte.

The CPU addresses the FDC to enable the data input buffers and sets the NWDS signal active to initiate a write transfer. The data byte on the Data Bus is loaded into the FDC, converted to a serial format, clock pulses added and, under control of the FDC transferred to the disc drive at the correct time tc ensure loading to the correct sector. When the data

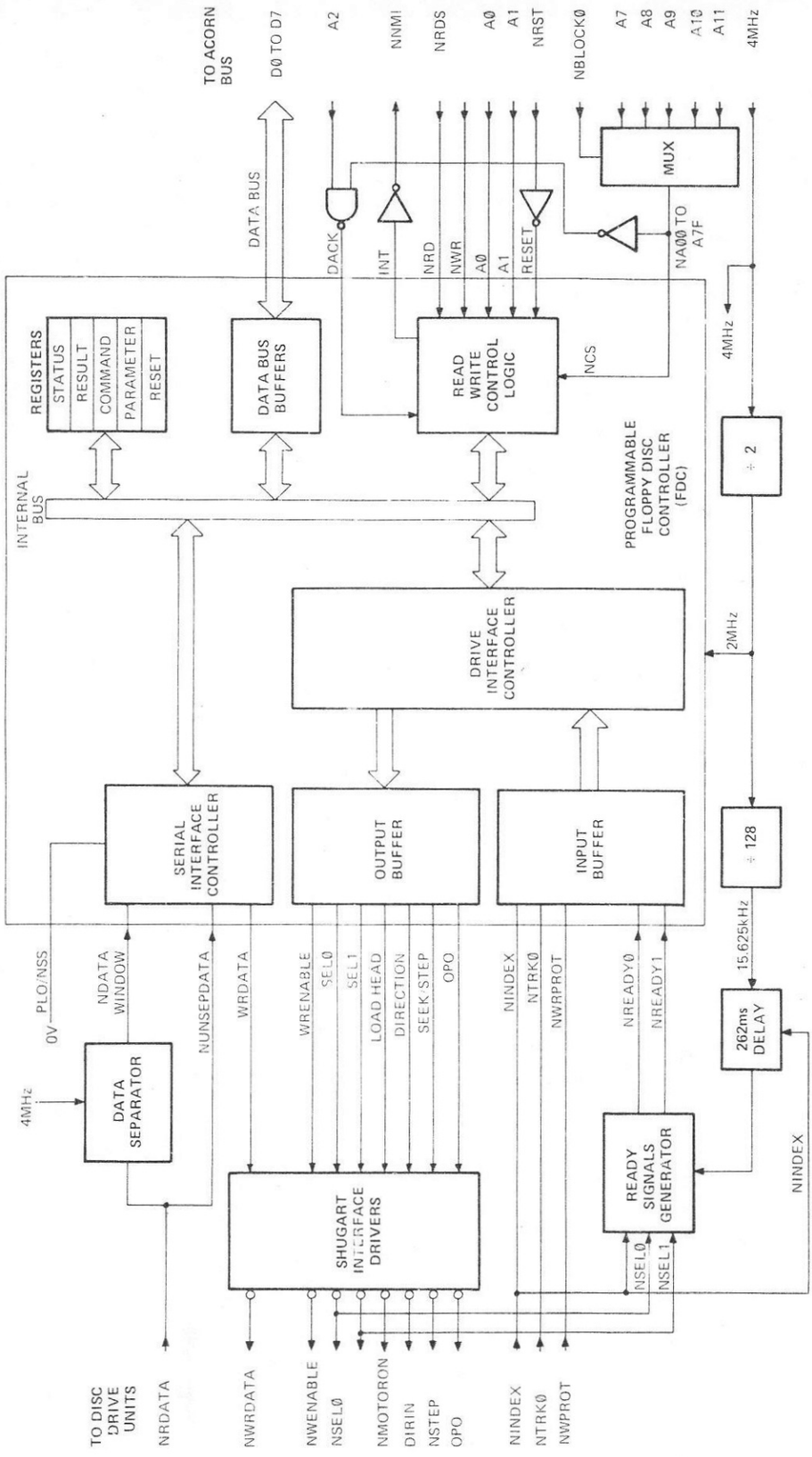


Figure 1. Floppy Disc Controller Block Diagram

byte has been transferred, the FDC flags the CPU (NNMI) to indicate that it is ready to receive the next data byte. The CPU reads the Status Register and the process is repeated for the remaining bytes of the data record. These transfers are synchronized by the FDC setting the NNMI interrupt flag active once every 64µs.

READ EXECUTE PHASE
The FDC searches for the required data record (defined by the command and parameter instructions). When the first byte is detected, it is read off the disc to the FDC which removes the clock pulses, converts it to a parallel form and flags the CPU using NNMI. The CPU reads the Status Register and then sets NRDS active enabling the transfer of the data byte onto the Acorn Bus. This procedure is repeated for each data byte with each data transfer between the disc, the FDC, and Acorn Bus being synchronized by NNMI once every 64µs.

RESULT PHASE
At the end of the Execute Phase, the Result Register Full bit is set in the Status Register, to indicate that the Command and Execute Phases of the data transfer have been completed.

During each data record transfer, the FDC maintains a tally on the number of data bytes transferred and any errors detected during the transfer. On completion of the data transfer, this data becomes valid in the Result Register. Following the next Status Register read operation, the CPU also reads the Result Register which indicates a successful completion of the command or, if not, the type of error or errors detected. These errors are more fully defined in Section 3.

When the Result Register has been read by the CPU, it is reset and the Status Register is updated to idle.

The FDC automatically unloads the disc head(s) if another command is not received from the CPU within ten revolutions of the disc (2s) after completion of a command.

1.3 LEADING PARTICULARS

1.3.1 Mechanical

Construction	:	Single Eurocard PCB
Size	:	100mm x 160mm

1.3.2 Power Supplies

+5V at 150mA.

1.3.3 Connections

Pin connections are given in Section 5.

Connectors : Double-sided edge connector to Acorn Bus. TTL signal levels are used, OV to +0.4V = logic 0, +2.4V to +5.25V = logic 1.

32-way ribbon cable to disc drive unit. TTL signal levels are used, OV to +0.4V = logic 0, +2.4V to +5.25V = logic 1. Outgoing signals are fed via drivers, providing up to 48mA at the logic 0 level.

2. CIRCUIT DESCRIPTION

The circuit diagram for the Floppy Disc Controller Board, Figure 8, is filed at the end of this section.

2.1 CPU INTERFACE

2.1.1 Addressing

The Floppy Disc Controller Board is addressed by the CPU on address lines A7 to A11 and the Block Ø signal $\overline{\text{ØXXX}}$. These signals are decoded by IC4 to provide the chip select signal $\overline{\text{AØØ–A7F}}$ to the FDC (IC1). $\overline{\text{AØØ–AFF}}$ is gated with address bit A2 at IC2/11 and IC2/8 to provide a second chip select signal, DACK, to the FDC.

2.1.2 Input/Output

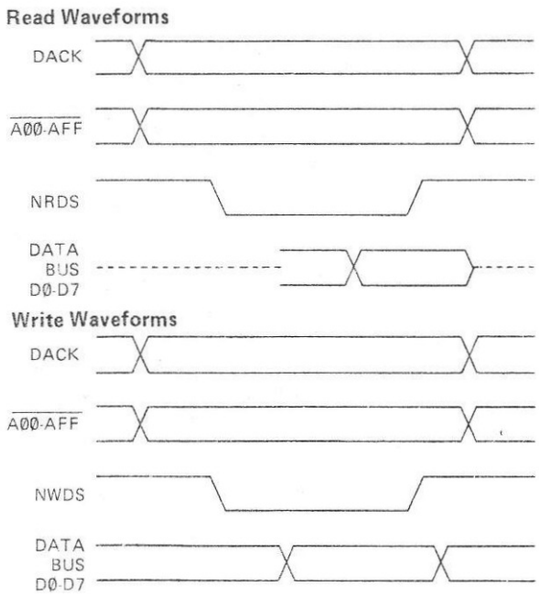
The transfer of data between the FDC and the CPU is controlled by the read and write signals NRDS and NWDS from the CPU. These signals set the direction of data transfer and synchronize the transfer to or from the data bus lines, D0 to D7 (Figure 2).

2.2 8271 FLOPPY DISC CONTROLLER

The internal structure of the Type 8271 FDC device, ICI is shown in block diagram form on Figure 1.

READ/WRITE CONTROL LOGIC
This logic provides address recognition from the CPU via address lines AØ to A2 and A7 to A11, the Block Ø signal $\overline{\text{ØXXX}}$ and the Read and Write signals NRDS and NWDS. Commands and any associated parameters on the data bus lines DØ to D7 are passed to the Serial and Drive Interface Controllers and the register via the internal bus.

This logic also generates the Interrupt signal INT (inverted by IC3 to produce NNW) when the FDC is ready to receive or transmit data over the Data Bus.



!

REGISTERS
The command and parameter data from the CPU, the status of the current data transfer, and the result of each transfer (successful or error detected) are held in these registers. The Status and Result Registers can be read by the CPU and the Reset Register set by a hardware or software Reset Command.

DRIVE INTERFACE CONTROLLER
This logic receives information on the type of transfer between disc and FDC (read or write) and the location of the data to be read or stored. This is transferred to the disc drive via output buffers.

It also receives status information from the disc drives, via input buffers, on the initial position of the disc drive head(s), NTRK0, write protected discs, NWRPROT, and the Index signal NINDEX. It also receives the Drive Ready signals NREADY0 and NREADY1 from the Ready signals generator. This information is used to control the transfer of data via the Serial Interface Controller.

SERIAL INTERFACE CONTROLLER
This logic provides the serial/parallel conversion of data between the 8-bit internal bus and the serial read and write lines to the Disc Drive as follows:

- Data to be written to disc is converted from an 8-bit parallel form to a serial stream with clock pulses. It is inverted and buffered by IC6/6 before being fed to the Disc Drive.
- Data read from disc consists of a serial stream with clock pulses. The Data Separator (Section 2. 4) provides timing pulses which enable the Serial Interface Controller to remove the clock pulses and convert the serial data to an 8-bit parallel form.

2.3 CLOCK SIGNALS

The timing for the Floppy Disc Controller Board is provided by the 4MHz clock input from the CPU Board, or may be provided by the local oscillator.

2.3.1 4MHz Operation

The 4MHz clock is divided by IC8 to provide a 2MHz clock signal to the FDC and by IC8 and IC9 to provide a 15.625kHz signal to the Ready Signals Generator Circuit.

2.3.2 Local Oscillator Operation

The 4MHz oscillator (IC13 and its associated components, is utilized when operation from the §2 signal is required. IC13/8, RV1, and C5 form a 4MHz, free-running oscillator. The 4MHz output is synchronized to the rest of the system timing by the §2 signal. This is inverted by IC13/6 and fed via the differentiating circuit of R9, R10 and C6 to trigger IC13/8 at every second cycle of the 4MHz output.

2.3.3 Local Oscillator Setting-Up Procedure

The local oscillator, IC13/8 is set up by adjusting RV1 to give an output of 4MHz.

The following equipment is required:

Dual-beam oscilloscope
Variable +5V power supply
Frequency Generator

Connect the oscilloscope Channel A to IC13 pin 8. Connect the oscilloscope Channel B and the frequency generator to Side A pin 29.

Set the oscilloscope to:

Amplitude	2V /cm
Timebase	100ns/cm
Trigger	Channel B

Connect the power supply to the board edge connector as follows:

+5V to Side .4 pin 1
0V to Side A pin 32

Set the power supply output to +5.0V.

Set the frequency generator to 1 MHz and at an output level which provides a useable display.

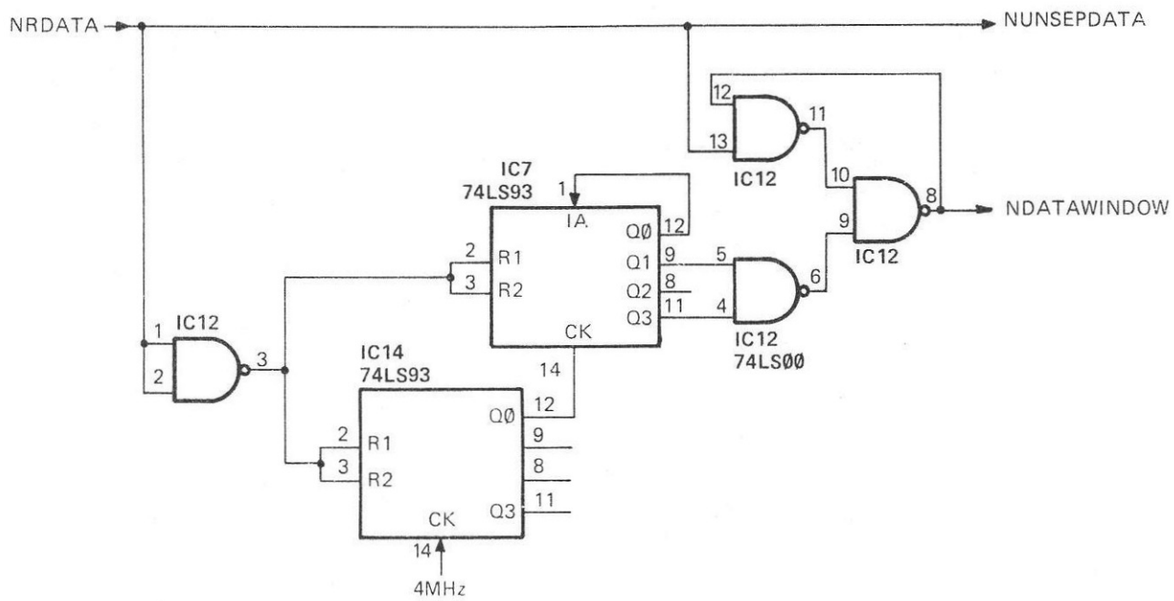
Adjust RV1 to give a stable 4MHz signal on IC13 pin 8 as seen on Channel A, in synchronization with Channel B.

In a 1MHz system the adjustment may be carried out using the system §2 clock signal instead of a signal generator.

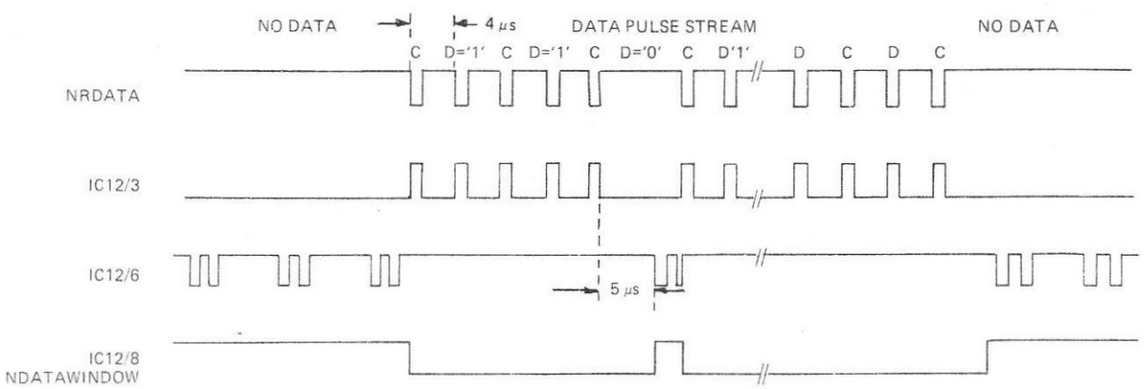
2.4 DATA SEPARATOR

The Data Separator Circuit is illustrated on Figure 3a. It provides identity pulses to the FDC, enabling it to extract the data bits from the combined clock and data pulse stream read off the disc.

The ripple counter, IC14 divides the 4MHz clock by 2 to provide a 2MHz clock signal to a second ripple counter, IC7. The ÷4 (pin 11) and ÷16 (pin 9) outputs of IC7 are NANDed by IC12/6 and inverted by IC12/8 to provide a positive going pulse to the FDC NDATAVVINDOW input once every 5µs in the absence of clock and data pulses on the Unseparated Data line (Figure 3b).



(a) Circuit



(b) Timing

Figure 3. Data Separator

The first dock pulse in a data byte from the disc resets the ripple counters. These counters are reset again by each data logic '1' bit and all the clock pulses, holding the output of the Data Separator Circuit low. Data logic '0' bits do not reset the counters via IC12/3. This allows the counters to run on, producing a positive-going pulse, to the FDC after 5µs. IC12/11 latches the positive-going NDATAWINDOW signals, until the negative-going edge of the next clock pulse. At the end of a data pulse stream, IC12/11 inhibits the negative-going NDATAWINDOW signal until the next data stream is received.

2.5 READY SIGNALS GENERATOR

This circuit produces a ready signal to IC1 to indicate that the selected drive has a disc fitted and is rotating at approximately the correct speed. (Figure 4).

The 4MHz clock is divided by 256 by the dual counter IC8. The resulting 15.625kHz output is fed to the 14-stage ripple counter IC9. Thus, after approximately 262ms from power on the count will have reached 4096 and the Q12 output of IC9 (pin 2) is high.

When a disc drive with a disc installed is switched on (SEL0 or SEL1), the first NINDEX pulse, inverted by IC2/6, resets IC9 to zero. Its Q12 output goes low and the count recommences. If the next NINDEX pulse arrives before the count reaches 4096 (less than 262ms), the low output from IC9 (Q12) is clocked through the dual bistable IC11 to produce NREADY0 for disc drive 1 or through IC10 to produce NREADY1 for disc drive 2.

This process continues while the disc drive is running at the correct speed to produce a continuous Ready signal. As soon as the disc drive is deselected, the appropriate Select signal goes high, setting the corresponding bistable IC10 or IC11, thus disabling the Ready signal.

2.6 FLOPPY DISC CONTROLLER/DRIVE INTERFACE

Unless stated otherwise, all signals are active low (0V). The signals from the FDC to the drive unit(s) are driven via open collector NAND buffer gates IC5 and IC6 to achieve the power requirements of the interface. Absolute timing of signals across this interface depends on the type of drive in use. Typical signal timings are given on Figures 5 and 6.

2.6.1 Outputs from Floppy Disc Controller

DRIVE SELECT — NSEL0 AND NSEL1
These two lines are multiplexed to provide control of up to four disc drive units. In this application NSEL0 and NSEL1 are used to select the one or two drives equipped.

NMOTORON
This signal, inconjunction with NSEL0 and NSEL1 switches on the d.c. drive motors in the disc drive units. Writing to and reading from the discs are delayed by 250ms after NMOTORON becomes

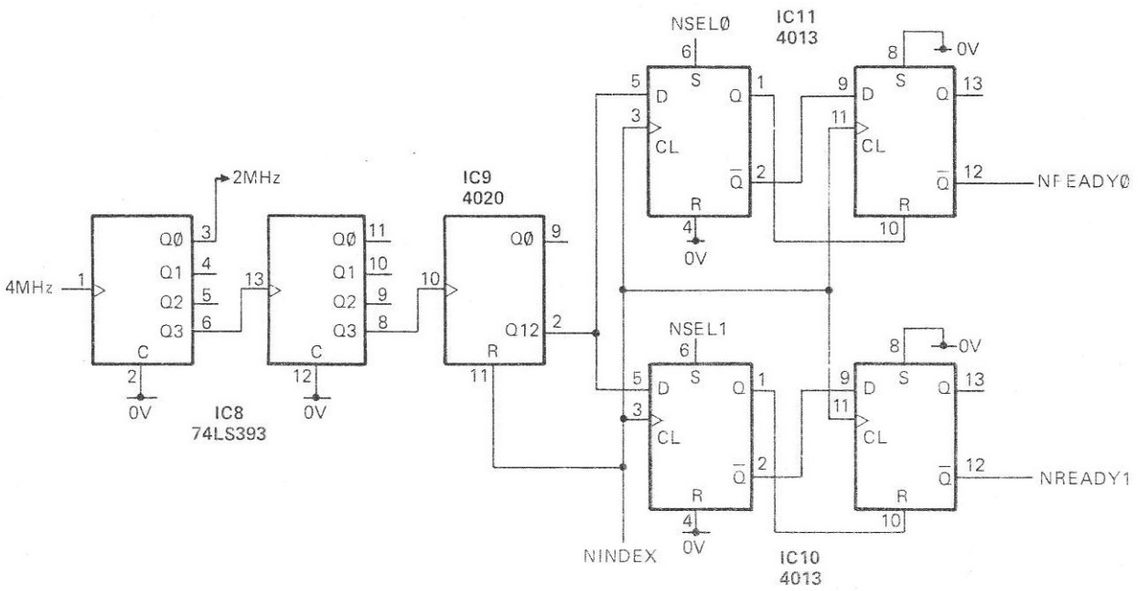
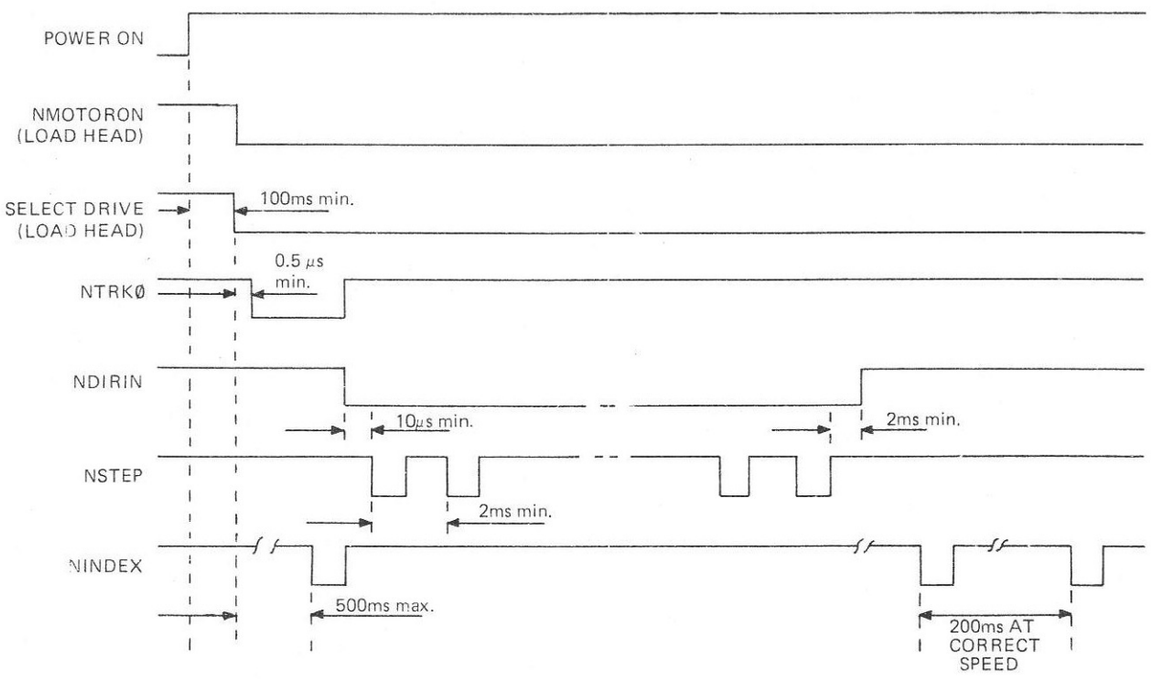
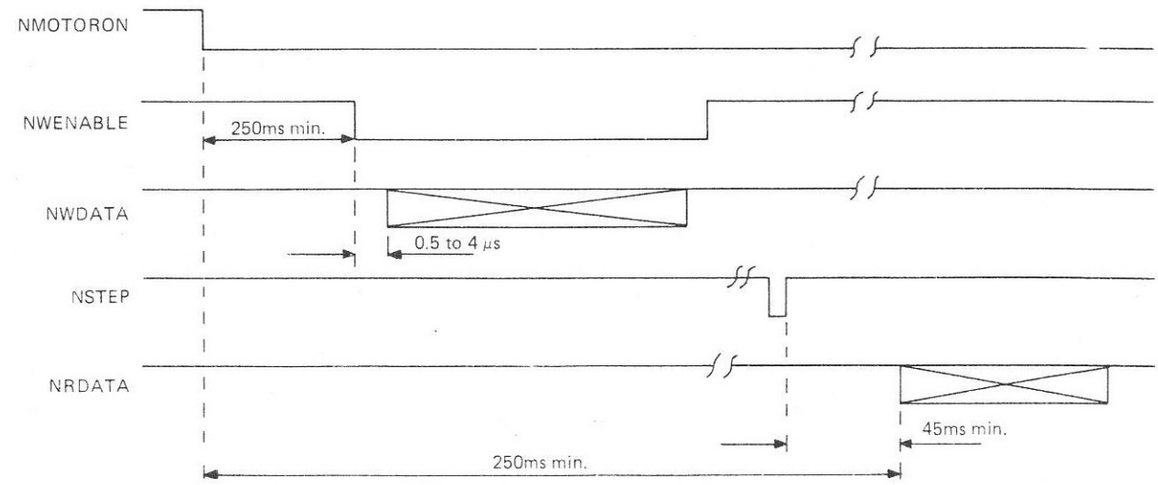


Figure 4. Ready Signals Generator



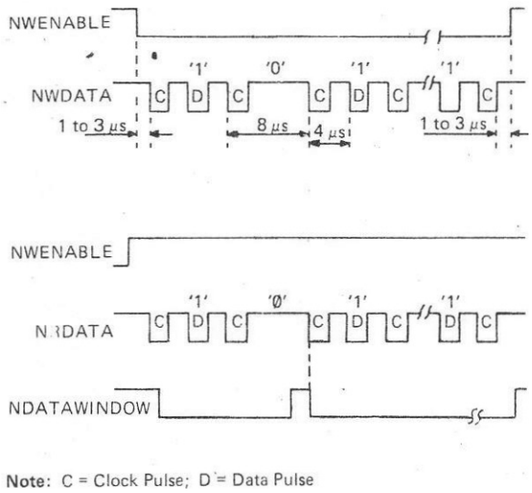
(a) Head Positioning



N.B. All timings quoted are typical and may vary between drive types.

(b) Write and Read

Figure 5. Drive Timing



Note: C = Clock Pulse; D = Data Pulse

Figure 6. Data Timing

active. During idle periods, 2s or more without a data transfer, the NMOTORON signal is disabled to increase motor life.

HEAD MOVEMENT DIRECTION — DIRIN
This Signal determines the direction of head movement when seeking a track. DIRIN low, in conjunction with NSTEP, causes the head to move towards the centre of the disc. DIRIN high and NSTEP cause the head to move out towards the edge of the disc.

NSTEP
Each negative-going, double NSTEP pulse causes the head to move one track position across the disc in the direction determined by the DIRIN signal.

READ/WRITE — NWENABLE
NWENABLE low enables the disc write circuits and, when high, enables the disc read circuits.

WRITE DATA — NWDATA
This line carries the serial write data to the disc drive units. Write data is enabled onto the selected disc drive unit by the NSEL0 and NSEL1 lines.

FAULT or OPO
This output is programmable by DOS to either reset a fault condition signalled by the disc drive or to select a disc surface on a double sided disc. In this application, it is used to select a disc surface. When FAULT is high, the left-hand surface (as viewed from the front of System 5) is selected: when low, FAULT selects the right-hand surface.

2.6.2 Inputs from Floppy Disc Drive Unit

TRACK 00 — NTRK0
This signal is low when the head is precisely positioned on track 00.

NINDEX
This line is pulsed low each time the disc index mark passes the index detector, once every 200ms. It should be noted that NINDEX is continuously active (low) while a disc is not fitted in the disc drive unit

READ DATA — NRDATA
This line carries the raw serial read data, that is unseparated clock and data signals. Signal NRDATA goes low for each 1 bit (clock and data) read off the disc.

WRITE PROTECT — NWPROT
The disc drive unit senses the insertion of a write protected disc and sets signal NWPROT low to prevent overwriting.

3. SOFTWARE PARAMETERS

The storage and retrieval of data on floppy disc is controlled entirely by the System 5 DOS supplied with the system. This control, the formatting of data, and the location of data on a particular disc is unalterable in use. Therefore only a brief description is given.

It should also be noted that the DOS resident in ROM supplied is specific to a particular manufacturer's disc drive unit and, that, where two disc drives are used, they must be of the same type and produced by the same manufacturer.

3.1. DOS

The operation of DOS (Disc Operating System) is fully described in the Disc Operating System document.

As soon as a disc drive with a disc loaded is selected, the disc catalogue held in Sectors 0 and 1 of Track 1 is loaded into the CPU's random access memory This catalogue information is assumed to be valid while the disc is rotating. If the disc drive is stopped and restarted for any reason (e.g. disc not required or for a change of disc) the catalogue for the disc in use is reloaded to RAM.

The catalogue contains the disc identity, and the names, size (number of bytes) and location (track and sector) of the files currently held on the disc; double-sided discs contain separate catalogues on each sur-

face. This enables the CPU to control efficiently the transfer of data (files) to and from disc without having to search the whole disc for a file or the next vacant file position.

3.2 ADDRESSING

The Floppy Disc Controller Board is addressed by the CPU at AØØ to A7F (hex) via address lines A7 to A11 and signal $\overline{0XXX}$. The various registers within the FDC device are accessed (command from CPU) using address lines AØ to A2 and the NRDS and NWDS signals as shown in Table 1. DACK corresponds to the chip select signal $\overline{AØØ–A7F}$ and A2, and NCS is the chip select signal $\overline{AØØ–A7F}$ generated from A7 to A11 and $\overline{0XXX}$.

NDACK	NCS	A1	AØ	NRDS	NWDS	OPERATION
1	Ø	Ø	Ø	Ø	1	Read Status
1	Ø	Ø	Ø	1	Ø	Write Command
1	Ø	Ø	1	Ø	1	Read Result
1	Ø	Ø	1	1	Ø	Write Parameter
1	Ø	1	Ø	1	Ø	Write Reset Reg.
Ø	1	X	X	1	Ø	Write Data
Ø	1	X	X	Ø	1	Read Data
Ø	Ø	X	X	X	X	Not Allowed

Table 1. FDC Addressing

Up to five command parameters are transferred over the data bus lines D0 to D7. These parameters further define the type of command and identify the required drive disc surface, track and sector, This information is decoded by the FDC to provide the drive and surface select signals SEL and OPO to the disc drives. Further decoding provides the head positioning control signals DIRIN (head direction) and STEP (head stepping) as required.

3.3 DISC FORMAT

The storage of data on floppy disc is organised by disc and surface, track and sector (Figure 7) as follows:

- *Disc (and disc drive).* Single or double-sided; one or both surfaces of a disc are used for recording data depending on the type of disc drive fitted.
- *Surface.* Each surface is formatted in 40 or 80 concentric tracks using the Utilities Disc FORM40 or FORM80 formatting program supplied depending on the type of disc drive in use.
- *Track.* Each track is organised in ten sectors. Track 0 is reserved for the Catalogue File and tracks 1 to 39 or 1 to 79 are used for data storage.
- *Sectors.* Each sector consists of identity and data fields. A data field holds up to 256 bytes of data. The sectors are recorded on a +3 stagger to obtain file transfers in the minimum number of disc revolutions (Figure 7).

Thus each surface can hold up to 100K bytes of data in 40 track format or 200K bytes of data in 80 track format.

Data is organized in files (data records) with up to 31 files to a disc surface. The number of files is limited by the size of the Catalogue to 31.

A file may be of any length up to the maximum capacity of the disc surface, A file always commences a the beginning of a sector and any unused space at the end of the last sector of a file is filled with random information.

The disc index hole together with a photo-electric detector in the disc drive provides the INDEX signal to the FDC once per disc revolution and also locates the beginning of the first sector on each track.

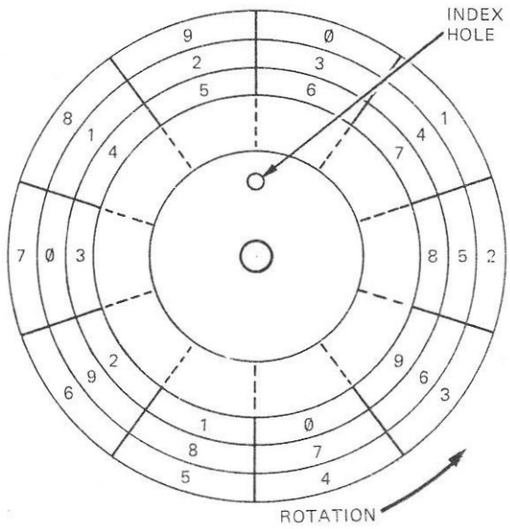


Figure 7. Data Format

3.4 DISC ERRORS

The FDC is capable of detecting many error conditions which could arise during the transfer of data to and from disc. These errors are interpreted by software which produces a disc error to the user, either on the VDU or printer, as shown in Table 2.

USER ERRORS			SYSTEM ERRORS		
Crunch	:	An attempt has been made to format a Write Protected disc.	Disc error Ø8	:	During a disc Read operation a clock bit was missing.
Disc Full	:	A block large enough to hold the file cannot be found. Periodic housekeeping with the COMPACT utility will minimise the occurrence of this error.	Disc error ØA	:	During a disc transfer the processor did not respond fast enough (probably due to a faulty Floppy Disc Interface Board).
Disc Prot	:	A Write operation has been attempted to a Write Protected disc.	Disc error ØC	:	The CRC (cyclic redundancy check) derived from the ID data read back, differed from that which was originally loaded to the disc.
Drive ?	:	Drive number is incorrrectly (or not specified.	Disc error ØE	:	The CRC derived from the data read back on a disc read differed from that loaded to the disc.
File ?	:	File name cannot be found.	Disc error 1Ø	:	During a transfer the disc stopped rotating (probably due to a badly inserted disc).
File Prot	:	A Write operation has been attempted to a Write Protected file.	Disc error 14	:	The Floppy Disc Controller Interface Board failed to find Track Ø. This error usually results from attempting to access an unformatted disc.
Full	:	31 files already exist on the current disc.	Disc error 18	:	The Floppy Disc Controller Interface Board failed to find the required sector. This error usually results from either using an unformatted disc, or the disc being corrupted by magnetic fields etc.
Syntax ?	:	Command is recognized but Syntax error exists.			

Table 2. Error Messages

4. FLOPPY DISC CONTROLLER CONNECTIONS

4.1 FLOPPY DISC CONTROLLER BOARD TO ACORN BUS

Pin	Mnemonic	Meaning	I/O
Side A			
1	+5V	+5V Line	I
2	A15	Address Lines 15 Not Used	I
3	A14		I
4	NWDS	Write Select	I
5	NRDS	Read Select	I
6	NRST	Reset	I
7	A8		
8	A7		
9	A6		
10	A5	Address Lines 6 5 4 3 Not Used	
11	A4		I
12	A3		
13	A2		
14	A1		
15	AØ		
16	D7		
17	D6		
18	D5		
19	D4		
20	D3	Data Lines	I/O
21	D2		
22	D1		
23	DØ		
24	A13		
25	A12	Address Lines 13 12 Not Used	
26	A11		I
27	A1Ø		
28	A9		
29	Φ2	System Φ2 Clock	I
30	R/NW	Read/Write Enable — Not Used	I
31	NBLOCKØ	Board Enable from CPU	I
32	0V	Earth	
Side B			
16	4MHz	4MHz Clock	I
29	NNMI	Interrupt from FDC	O

4.2 FLOPPY DISC CONTROLLER BOARD TO FLOPPY DISC DRIVE (DAISY CHAINED TO ALL DRIVES)

Pin	Mnemonic	Meaning	I/O
2	—	—	—
4	—	—	—
6	—	—	—
8	NINDEX	Index Signal from Drive	I
1Ø	NSELØ	Multiplexed Drive Select Signals (1 of 4)	O
12	NSEL1		
14	—	—	—
16	NMOTORON	Motor Drive Enable	O
18	DIRIN	Head Movement Direction	O
20	NSTEP	Moves Head 1 Track in Direction Set by DIRIN	O
22	NWDATA	Data to Disc	O
24	NWENABLE	Enable Disc Write Circuits Enables Disc Read Circuits when High	O
26	NTRKØ	Indicates Head is precisely positioned on Track ØØ	I
28	NWPROT	Disc is Write protected	I
30	NRDATA	Data from Disc	I
32	OPO	Selects Disc Surface for Double Sided Drives. User Programmable.	O
34	—	—	—

Odd numbered Pins connected to Earth.

5. PARTS LIST

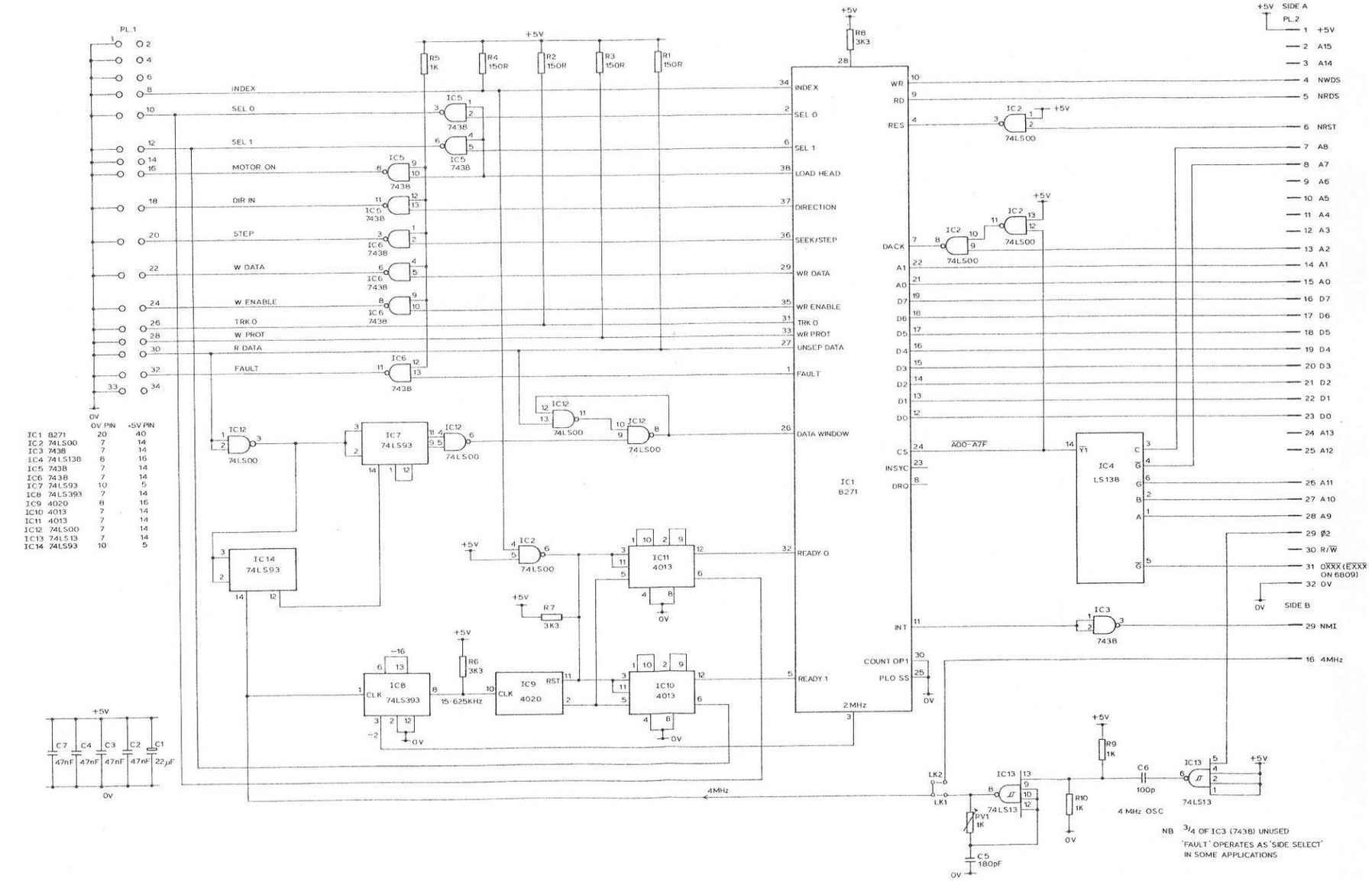
5.1 MECHANICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
	Printed Circuit Board, 200.004		1	
	Connector, 34-way		1	
	Connector, 64-way		1	
	40-pin IC Socket		1	
	16-pin IC Socket	2		
	14-pin IC Socket	10		

5.2 ELECTRICAL PARTS

ITEM	DESCRIPTION	VALUE	QTY	PART NO.
C1	Capacitor	15µF	1	
C2...C4	Capacitor	47nF	3	
C5	*Capacitor	180pF	1	
C6	*Capacitor	100pF	1	
C7	Capacitor	47nF	1	
IC1	Integrated circuit	8271	1	
IC2	Integrated circuit	74LS00	1	
IC3	Integrated circuit	7438	1	
IC4	Integrated circuit	74LS138	1	
IC5,IC6	Integrated circuit	7438	2	
IC7	Integrated circuit	74LS93	1	
IC8	Integrated circuit	74LS393	1	
IC9	Integrated circuit	4020	1	
IC10,IC11	Integrated circuit	4013	2	
IC12	Integrated circuit	74LS00	1	
IC13	*Integrated circuit	74LS13	1	
IC14	Integrated circuit	74LS93	1	
R1.:.R4	Resistor	150	4	
R5	Resistor	1K	1	
R6...R8	Resistor	3K3	3	
R9, R10	*Resistor	1K	2	
RV1	* Resistor, variable	1K	1	

*These components are not used in the Acorn System 5 application.



	0V PIN	+5V PIN
IC1 8271	20	40
IC2 74LS00	7	14
IC3 7438	7	14
IC4 74LS138	8	16
IC5 7438	7	14
IC6 7438	7	14
IC7 74LS93	10	5
IC8 74LS393	7	14
IC9 4020	8	16
IC10 4013	7	14
IC11 4013	7	14
IC12 74LS00	7	14
IC13 74LS13	7	14
IC14 74LS93	10	5

Figure 8 Floppy Disc Controller Circuit Diagram